IN THE CLAIMS:

Please amend the claims as indicated below.

1. (Amended) A bidirectional bus repeater circuit, comprising:

a connector to a first segment of a bidirectional bus;

a connector to a second segment of a bidirectional bus; and

a pair of buffers for each bit on said bidirectional bus, each buffer in said pair transferring data in a given direction between said first segment and said second segment of ~~on~~ said bidirectional bus ~~based on a direction control signal~~ ; and

a pair of indicator lines, wherein a single voltage change on one of said indicator lines causes one or more of said pair of buffers to transfer data in a given direction for a finite period of time.

2. (Amended) The repeater of claim 1, further comprising an additional pair of buffers associated with ~~a~~ said pair of indicator lines controlling said direction of said bidirectional bus ~~control signal~~.

3. (Amended) The repeater of claim 1, further comprising a direction control block that controls said direction of said bidirectional bus ~~control signal~~ based on activity on one of ~~an~~ said indicator lines associated with said bidirectional bus.

4. (Amended) The repeater of claim 3, wherein a given node connected to said bidirectional bus must toggle one of said pair of indicator lines in order to drive said bidirectional bus.

5. (Cancelled) The repeater of claim 3, wherein a given node connected to said bidirectional bus must toggle said indicator line in order to drive said bidirectional bus.

6. (Cancelled) The repeater of claim 1, wherein said direction control signal indicator signals is activated upon a change of voltage on an indicator line associated with one of said segments of said bus to enable said corresponding buffers.

7. (Amended) The repeater of claim 1, wherein one of said ~~direction control signal~~ pair of indicator lines continues to enable said corresponding buffers until the second of said bus segments reaches the same logic level as the first of said bus segments.

8. (Amended) A bidirectional bus, comprising:

a first segment connected to one or more nodes;

a second segment connected to one or more nodes; ~~and~~

a bidirectional bus repeater having a pair of buffers for each bit on said bidirectional bus, each buffer in said pair transferring data in a given direction between said first segment and said second segment of ~~on~~ said bidirectional bus ~~based on a direction control signal;~~ and

a pair of indicator signals, wherein a single voltage change on one of said indicator signals causes one or more of said pair of buffers to transfer data in a given direction for a finite period of time.

9. (Amended) The bidirectional bus of claim 8, wherein said bidirectional bus repeater further comprises an additional pair of buffers associated with said ~~a~~ pair of indicator signals ~~lines~~ controlling said direction of said bidirectional bus ~~control signal~~.

10. (Amended) The bidirectional bus of claim 8, wherein said bidirectional bus repeater further comprises a direction control block that controls said direction of said bidirectional bus ~~control signal~~ based on activity on ~~an~~ said pair of indicator ~~line~~ signals associated with said bidirectional bus.

11. (Amended) The bidirectional bus of claim 10, wherein a given node connected to said bidirectional bus must toggle one of said indicator ~~line~~ signals in order to drive said bidirectional bus.

12. (Amended) A method for repeating a signal on a bidirectional bus, comprising the steps of:

connecting two segments of said bidirectional bus;

providing a pair of buffers for each bit on said bidirectional bus; and

transferring a bit of data in a given direction through one of said pair of buffers based on ~~a direction control signal~~ a pair of indicator signals, wherein a single voltage change on one of said indicator signals causes one or more of said pair of buffers to transfer data in a given direction for a finite period of time.

13. (Amended) The method of claim 12, wherein said bidirectional bus comprises an additional pair of buffers associated with ~~a~~ said pair of indicator ~~lines~~ signals controlling said direction of said bidirectional bus ~~control signal~~.

14. (Amended) The method of claim 12, wherein a direction control block controls said direction of said bidirectional bus ~~control signal~~ based on activity on ~~an~~ said pair of indicator ~~line~~ signals associated with said bidirectional bus.

15. (Amended) The method of claim 12, wherein a given node connected to said bidirectional bus must toggle one of said pair of indicator ~~line~~ signals in order to drive said bidirectional bus.